ABSTRACT OF THE DISCLOSURE

An 1 bit memory cell MC is composed of one MOS transistor having a floating bulk region which is electrically isolated from others. A gate electrode 13 of the MOS transistor is connected to a word line WL, a drain diffusion region 14 thereof is connected to a bit line BL, and a source diffusion region 15 thereof is connected to a fixed potential line SL. The memory cell stores a first threshold state in which majority carriers produced by impact ionization are injected and held in the bulk region 12 of the MOS transistor and a second threshold state in which the majority carriers in the bulk region 12 of the MOS transistor are emitted by a forward bias at a pn junction on the drain side as binary data. Thereby, a semiconductor memory device in which a simple transistor structure is used as a memory cell, enabling dynamic storage of binary data by a small number of signal lines can be provided.